Electronics Circuits

Single Stage and Multistage Amplifiers

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Single Stage & Multi Stage Amplifiers

In this module we will discuss small signal BJT amplifiers. An amplifier circuit can be analyzed in two ways :

(i) By drawing its equivalent circuits

(ii) By graphical method

EQUIVALENT CIRCUITS OF TRANSISTOR AMPLIFIER

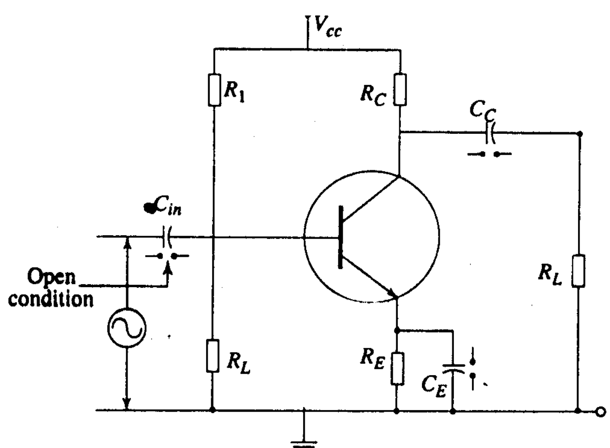
Analysis of an amplifier is easily done by drawing its equivalent circuit. While working, an amplifier has both D.C. as well as A.C. conditions. The D.C. biasing produces D.C. currents and voltages while A.C. signal produces A.C. currents and voltages. Accordingly an amplifier will have two equivalent circuits, viz. D.C. equivalent circuit and A.C. equivalent circuit.

D.C. Equivalent Circuit

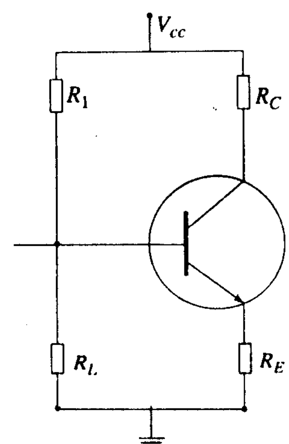
While drawing D.C. equivalent circuit, assume that

- Only D.C. conditions are prevailing, i.e. the amplifier has been biased and A.C. signal is not applied. All A.C. sources, therefore, are to be removed.
- D.C. can not flow through capacitors which produce infinite impedance for D.C. In other words, capacitors are open circuited for D.C., i.e. all capacitors should be removed.

Keeping the above in mind, the remaining circuit shall be the D.C. equivalent circuit. Naturally, the D.C. equivalent circuit shall be nothing but the biasing circuit and the transistor itself.



(a) Amplifier circuit



(b) DC equivalent Circuit

Figure (a) shows the amplifier circuit. Figure (b) shows its D.C. equivalent circuit.

A.C. Equivalent Circuit

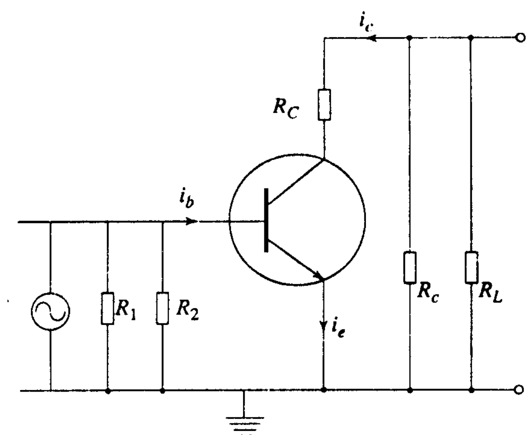
While drawing A.C. equivalent circuit of an amplifier proceed in just the reverse way to that of (I) above.

(a) Assume that only A.C. conditions prevail; hence remove the D.C. biasing and show the A.C. signal applied at the input of the amplifier.

(b) Now A.C. can easily flow through the capacitor as the later acts just a short circuit for the A.C.

In other words, capacitors are to be replaced by a short circuiting resistance of the negligible resistance.

By doing so, the amplifier will be reduced to it's A.C. equivalent circuit, in which R_1, R_L ,R_C and R_2 will come in parallel to one another (see figure).



A.C. equivalent circuit of amplifier

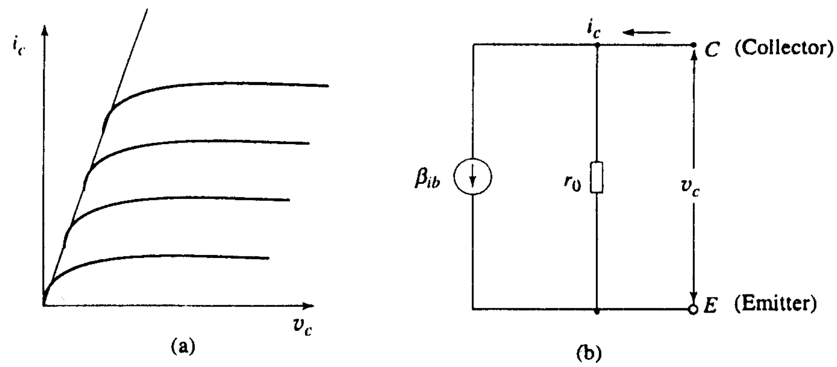
Alternative AC Equivalent Circuits for the Amplifier. Strictly speaking, we are more interested in the A.C. equivalent circuit of the amplifier, as we have to calculate A.C. current gain, voltage gain, A.C. power gain, etc. For drawing another A.C. equivalent circuit, we shall proceed in steps :

Step 1 : A.C. equivalent circuit for output side. For drawing A.C. equivalent circuit for output (collector emitter) side, proceed as under

(i) Looking at the output characteristics of the transistor, we can see that the output current I_c remains almost constant (Figure a); hence replace the transistor (of figure given above) by a constant source; having its output impedance (which is very high in MΩ) in parallel.

(ii) Remove D.C. supplies(biasing) as we are to study only it's A.C. behaviour.

(iii) The capacitors provide a short circuit path for A.C. Hence replace capacitors by resistors of negligible resistance. Figure b shows A.C. equivalent circuit for output side of the amplifier.



Step 2 : A.C. equivalent circuit for input side of the amplifier

(i) Looking at the input characteristic of the transistor (Figure a) we see that it is just the same as that of a forward biased diode. The value of the input junction resistance (r_I) is also very small (about 750 Ω).

(ii) Remove D.C. supplies

(iii) Replace capacitors by short circuiting lines

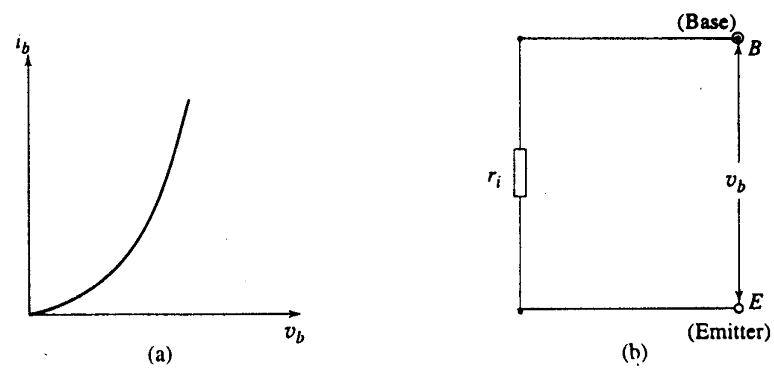
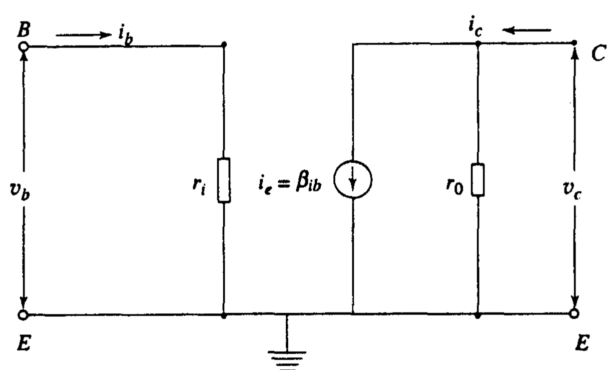


Figure (b) shows the A.C. equivalent circuit for input side.

Given figure shows complete A.C. equivalent circuit of the amplifier by combining the equivalent circuits for its output and input sides.



GRAPHICAL METHOD – DRAWING LOAD LINES

For analyzing an amplifier circuit by the graphical method, we draw load lines. An amplifier has D.C. as well as A.C. conditions, accordingly it has two load lines :

- D.C. load line
- A.C. load line

D.C. Load Line

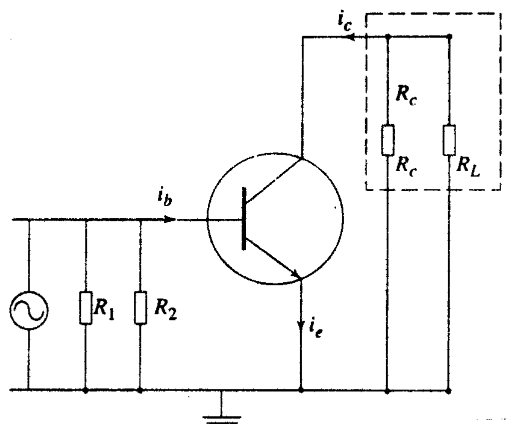
Already discussed.

A.C. Load Line

The line drawn on the output characteristic of an amplifier when A.C. conditions prevail (i.e. with signal applied) is called an "A.C. load line".

For drawing A.C. load line, again we have to find two end points of maximum V_{CE}(on voltage axis) and maximum I_C(on current axis). Joining these two, we get an A.C. load line.

(i) Under the application of A.C. signal, referring to the A.C. equivalent circuit (Figure) resistance R_C appears parallel to the load R_L.



The total A.C. Load = $R_{AC} = R_C \| R_L = \dfrac{R_C R_L}{R_C + R_L}$

(ii) When A.C. signal is applied, it produces a change(swing) in the position of Q point above and below the load line.

Maximum collector current due to A.C. signal = I_C

Maximum swing(positive) of A.C. collector emitter voltage = I_C x R_{AC}

Hence Total maximum collector emitter voltage = $V_{CE} + I_C R_{AC}$

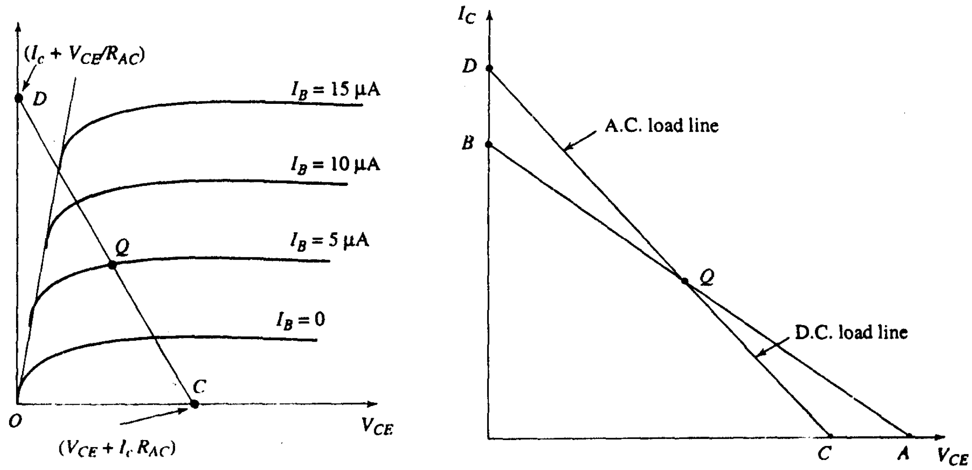
Where V_{CE} is the collector emitter voltage in D.C. conditions and R_{AC} is the A.C. load [i.e. $R_C R_L/R_C + R_C$]

This gives the first point (C) of the load line on the voltage axis.

(iii) Maximum swing(positive) in the A.C. collector current = V_{CE}/R_{AC}

Hence total maximum collector current = $I_C + V_{CE}/R_{AC}$

This gives point D of the load line on current axis.



(a) **(b)**

Now CD is the A.C. load line (see figure a). The Q-point can also given by the intersection of D.C. and a.C. load lines (see figure b).

Current, Voltage and Power Gains

An amplifier is used to raise the strength of a weak A.C. signal, we are interested in the various gains of the device. For this purpose only A.C. quantities will be considered.

Current Gain(C.G.). The "current gain" of an amplifier is defined as the ratio of A.C. output collector current to the A.C. input base current. Hence C.G.

$\beta_{AC} = A_I$ = A.C. output collector current/A.C. input base current

i.e. β_{AC} or $A_I = I_c/i_b$

Voltage Gain(V.G.). The voltage gain of an amplifier is defined as the ratio of output A.C. voltage to the input A.C. voltage.

$$\text{V.G.} = A_v = \frac{\text{output AC voltage}}{\text{input AC voltage}} = \frac{\text{output AC current x load resistance}}{\text{input AC current x input resistance}}$$

$$= \frac{i_c.R_{AC}}{i_b.R_{in}} = \beta.\frac{R_{AC}}{R_{in}} = A_i = \frac{R_{AC}}{R_{in}}$$

where R_{AC} = total effective load resistance found from AC equivalent circuit of the amplifier i.e. $R_{AC} = R_C||R_L = R_CR_L/R_C+R_L$.

R_{in} = Input junction resistance of the transistor, i.e. $R_{in} = \Delta V_{BE}/\Delta I_B$

Power Gain(P.G.). The "power gain" of an amplifier is defined as the ratio of output AC power across the load to the input AC power of the signal.

$$P.G. = A_p = \frac{\text{output AC power}}{\text{input AC power}} = \frac{(\text{output AC current})^2.(\text{load resistance})}{(\text{input AC current})^2.(\text{input resistance})}$$

$$= \frac{i_c^{\ 2}.R_{AC}}{i_b^{\ 2}.R_{in}} = \left(\frac{i_c^{\ 2}}{i_b^{\ 2}}\right).\frac{R_{AC}}{R_{in}} = \beta^2.\frac{R_{AC}}{R_{in}}$$

$$= A_i^{\ 2}.\frac{R_{AC}}{R_{in}} = A_i\left(A_i.\frac{R_{AC}}{R_{in}}\right)$$

Or Power gain = current gain x voltage gain

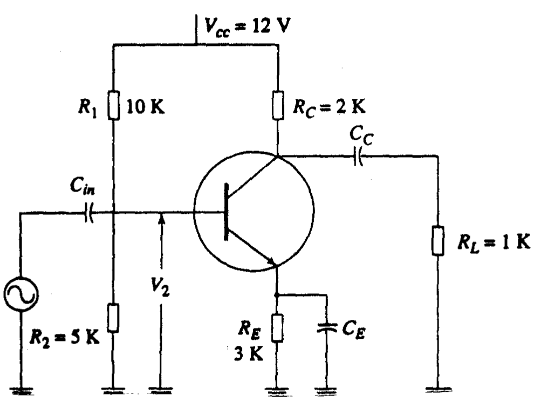
Example

The amplifier circuit (See figure (a)) has $R_1 = 10\ \Omega$, $R_2 = 5$ K, $R_C = 2$ K, $R_E = 3$ K and $R_L = 1$ K. Assume the transistor to be of silicon and $V_{CC} = 12$ V. Do the following:

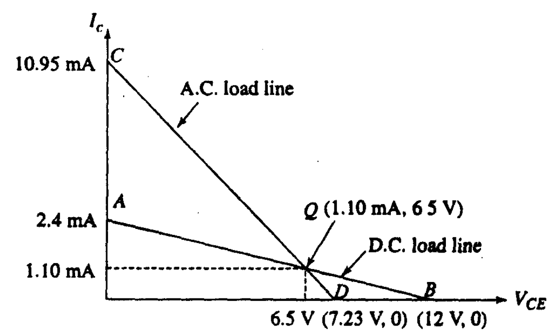
- *(i) Draw D.C. load line*
- *(ii) Locate the Q point*
- *(iii) Draw A.C. load line*

Solution

See figure (b).



(a)



(b)

(i) **DC load line**

Taking the output equation for the amplifier

$V_{CC} = V_{CE} + I_CR_C + I_ER_E$

$V_{CC} = V_{CE} + I_CR_C + I_CR_E \quad (I_E \approx I_C)$

If $I_C = 0$

$V_{CC} = V_{CE} = 12$ V.

This gives point B (12 V, 0), on voltage axis (See figure b). If V_{CE} = 0, the above equation is reduced to

$$V_{CC} = 0 + I_C R_C + I_C R_E = I_C(R_C + R_E)$$

Or $$I_{CC} = \frac{V_{CC}}{R_C + R_E} = \frac{12V}{(2+3)K} = 2.4mA$$

This gives point A (0,2.4 mA) on the current axis. Join A and B, the line AB will be required D.C. load line.

(ii) **To locate Q-point**

Apply potential divider theorem in the series circuit of R_1 and R_2

Voltage across R_2 is

$$V_2 = V_{CC}/(R_1 + R_2)R_2 = [12\text{ V}/(10+5)\text{K}]\text{x}5\text{K} = 4\text{ V}$$

Now $$V_2 = V_{BE} + I_E R_E \approx V_{BE} + I_C R_E \qquad (I_E \approx I_C)$$

$$4\text{ V} = 0.7\text{ V} + I_C.3\text{K}$$

$$I_C = (4\text{ V} - 0.7\text{ V})/3\text{ K} = 1.10\text{ mA}$$

Now again using output equation

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 12\text{ V} - 1.10(2 + 3)\text{ K}$$

$$V_{CE} = 6.5\text{ V}.$$

The coordinates of Q-point are (1.10 mA, 6.50 V) .

(iii) **To draw AC load line**

Effective(total) load resistance (from AC equivalent circuit)

$$R_{AC} = \frac{R_C.R_L}{R_C + R_L} = \frac{2x1}{2+1} = \frac{2}{3} = 0.66K$$

Maximum collector emitter voltage = $V_{CE} + I_C R_{AC}$ = 6.5 V + 1.10(0.66K)V = 7.23 V

This gives point D(7.23 V, 0) on the voltage axis.

Maximum collector current = $I_C + V_{CE}/R_{AC}$ = 1.10 + 6.5/0.66 K = 10.95 mA

This gives point C (0, 10.95 mA) on current axis.

Join C and D, CD is the AC load line.

Note : The intersection of DC and AC load lines shall give the Q-point automatically.

Example

In an amplifier, when the signal changes by 0.04 V, the base current changes by 15 μA and collector current changes by 2 mA. If R_L = 10 K and R_C = 8 K, find:

(i) *Current gain*

(ii) *Input impedance*

(iii) *AC load*

(iv) *Voltage gain*

(v) *Power gain*

Solution

Given ΔV_{BE} = 0.04 V (change in signal)

ΔI_B = 15 mA

ΔI_C = 2 mA

R_L = 10 K

R_C = 8 K

(i) Current gain = β or $A_I = \Delta I_C/\Delta I_B$ = 2 mA/15 μA = 2 x 10^3/15 μA = 133.33 .

(ii) Input impedance = $R_{in} = \Delta V_{BE}/\Delta I_B$ = 0.02 V/15 μA = 0.02 V/(15 x 10^{-6} A) = 1.33 K

(iii) A.C. load $R_{AC} = R_C.R_L/(R_C + R_L)$ = 8 x 10/(8 + 10) = 4.44 K

(iv) Voltage gain $A_v = A_I$ x (R_{AC}/R_{in}) = 133.33 x 4.44 K/1.33 K = 445.10 $(A_I = \beta)$

(v) Power gain $A_p = A_I$ x A_v = 133.33 x 445.10 = 59345.18

Hybrid Parameters

Usually an amplifier is analyzed with the help of β and other parameters. Though this method is simple, but very accurate results are not obtained. The reason is that for the analysis, the input and the output circuits of an amplifier are considered to be completely independent, but in practice it is not so.

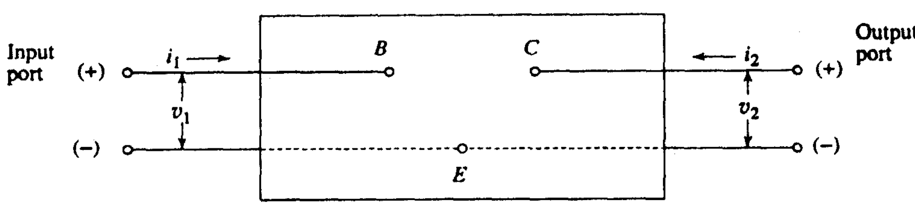
Therefore, for analyzing the behaviour of amplifiers, "hybrid method" is used which gives the most accurate results.

ADVANTAGES OF HYBRID PARAMETERS

- They give accurate results as the interactions of input and output circuits of the amplifier have been taken into account.
- These parameters can be measured easily.

TWO-PORT NETWORK

A transistor is a three terminal(Emitter E, Base B, Collector C) device. In all the three configurations one of the three terminals is common to input and output circuits, so there are **two-ports**(pair of terminals) in a transistor circuit. Therefore, it can be considered as a two port network for discussion (See figure).



Transistor as port

The voltages and currents of the above port can be related by the following equations

$$v_1 = h_{11}i_1 + h_{12}v_2 \quad \text{(i)}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \quad \text{(ii)}$$

Here h_{11},h_{21},h_{12} and h_{22} are constants and are known as "**hybrid parameters**".

UNITS FOR H-PARAMETERS

h_{11}	ohm
h_{12}	no units
h_{21}	no units
h_{22}	mho i.e. 1/ohm

DETERMINATION OF H-PARAMETERS

For the determination of h-parameters, proceed as follows:

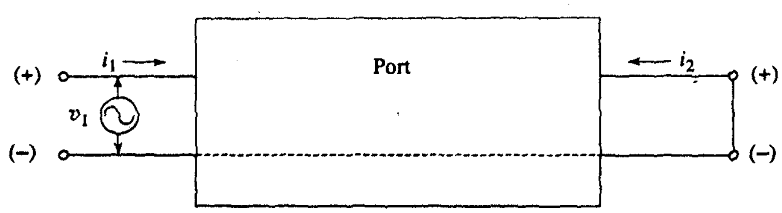
Short circuit the output terminals (See figure)

(a) Now the output voltage $v_2 = 0$, putting the value in Equation (I) above

$$v_1 = h_{11}i_1 + h_{12}0$$

$$h_{11} = v_1/i_1$$

h_{11} is called **input impedance**.



(b) Putting $v_2 = 0$ in equation(ii)

$$i_2 = h_{21}.i_1 + h_{22}.0$$

$$h_{21} = i_2/i_1$$

h_{21} is called "current gain" or "**forward current ratio**".

Open circuit the input terminals (See Figure)

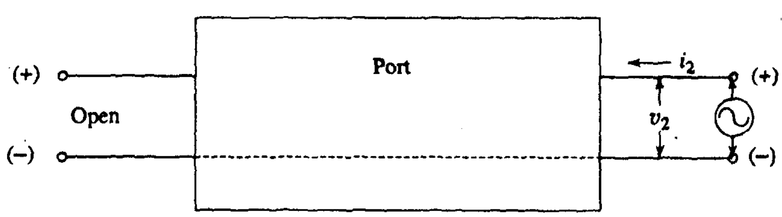
(a) This will reduce input current to $i_1 = 0$

Putting $i_1 = 0$ in Equation (I)

$$v_1 = h_{11}.0 + h_{12}.v_2$$

$$h_{12} = v_1/v_2$$

h_{12} is called "**reverse voltage ratio**" or "feedback voltage ratio".



(b) Putting $i_1 = 0$ in Eq. (ii)

$$i_2 = h_{21}.0 + h_{22}.v_2$$

$$h_{22} = i_1/v_2$$

The h_{22} is called "**output admittance**"(reverse of resistance).

Now the various h-parameters can be defined as :

$h_{11} = v_1/i_1$ ($v_2 = 0$) = input impedance (with output shorted = h_i (in ohms)

$h_{21} = i_2/i_1$ ($v_2 = 0$) = forward current ratio (with output shorted) = h_f (no units)

$h_{12} = v_1/v_2$ ($i_1 = 0$) = reverse voltage ratio (with input open) = h_r (no units)

$h_{22} = i_1/v_2$ ($i_1 = 0$) = output admittance (with input open) = h_0 (in mho)

NOMENCLATURE OF H-PARAMETERS FOR COMMON EMITTER CONFIGURATION

h_{11} h_{ib}

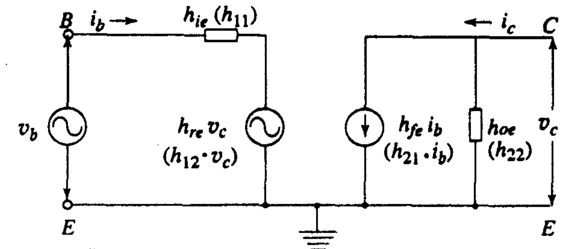
h_{12} h_{rb}

h_{21} h_{fb}

h_{22} h_{ob}

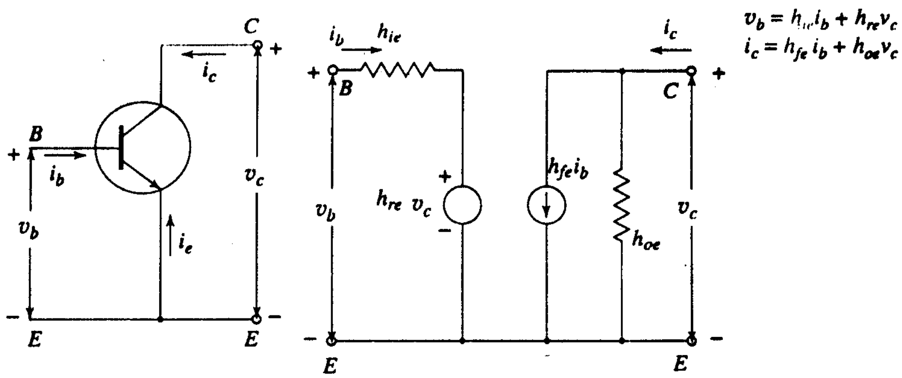
LOW FREQUENCY TRANSISTOR HYBRID MODEL

Following figure shows hybrid model of a transistor in CE configurations.



Hybrid model of transistor in CE configurations

Following figure shows circuit arrangement, hybrid model and V-I equations for CE configurations for an N-P-N transistor.



Circuit, hybrid model and V-I equations for N-P-N transistor (CE configuration)

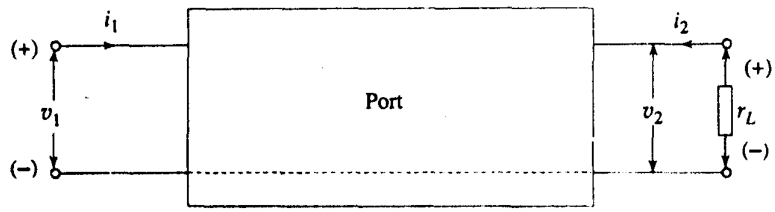
The circuit and equations shown in the figure are valid either for N-P-N or P-N-P transistors and independent of the type of load or method of biasing.

Performance of a Transistor in h-Parameters

We shall study the performance of a transistor in CE configuration in respect of its :

- Input impedance

- Current gain
- Voltage gain
- Power gain
- Output admittance



Input Impedance (Z_{in}). The input impedance is the ratio of input voltage to the input current.

In figure, input voltage is v_1 and input current is i_1. The input impedance

$$Z_{in} = v_1/i_1 \qquad \text{(i)}$$

We know, in terms of h-parameters

$$v_1 = h_{11}.i_1 + h_{12}.v_2$$

Hence putting the value of v_1 in Eq. (i)

We get

$$Z_{in} = \frac{h_{11}.i_1 + h_{12}.v_2}{i_1} = h_{11} + \frac{h_{12}.v_2}{i_1} = h_{11} + h_{12}.\frac{v_2}{i_1}$$

Further, in terms of h-parameters

$$i_2 = h_{21}.i_1 + h_{22}.v_2 \qquad \text{(ii)}$$

If A.C. load resistance is r_L, $i_2 = -v_2/r_L$ the minus sign is used to indicate that the direction of i_2 is opposite to the marked direction.

Putting value of i_2 in Eq. (ii) we get

$$-v_2/r_L = h_{21}.i_1 + h_{22}.v_2$$

or $$- h_{21}.i_1 = v_2(h_{22} + 1/r_L)$$

or $$\frac{v_2}{i_1} = \frac{-h_{21}}{h_{22} + 1/r_L} \qquad \text{(iii)}$$

Again, substituting this value in the expression for Z_{in}, we got above

$$Z_{in} = h_{ie} - \frac{h_{re}.h_{fe}}{h_{oe} + 1/r_L}$$

You are advised to write expression of Z_{in} also for CB and CC configuration.

Current Gain (A_I). Current gain is the ratio of output current to input current.

See figure above.

$A_i = i_2/i_1$ (iv)

Now $i_2 = h_{21}.i_1 + h_{22}.v_2$ (in terms of h parameters)

$= h_{21}.i_1 + h_{22}(-i_2r_1)$ ($v_2 = -i_2r_L$)

or $i_2 = h_{21}.i_1 - h_{22}.r_L.i_2$

or $i_2(1+h_{22} \text{ x } r_L) = h_{21}.i_1$

or $$\frac{i_2}{i_1} = \frac{h_{21}}{1+h_{22}xr_L} \quad \text{(v)}$$

or $$A_i = \frac{h_{21}}{1+h_{22}xr_L}$$

Substituting the values in h-parameters in CE configuration,

$$A_i = \frac{h_{fe}}{1+h_{oe}.r_L}$$

If $h_{oe}.r_L << 1$ then current gain = h_{fe}.

Voltage Gain (A_v). The voltage gain is the ratio of output voltage to input voltage.

Refer above figure again

$A_v = v_2/v_1$ (vi)

From input circuit

$Z_{in} = v_2/i_1$ or, $v_1 = i_1.Z_{in}$

Thus $A_v = v_2/i_1.Z_{in} = (v_2/i_1)(1/Z_{in})$ (vii)

Now $$\frac{v_2}{i_1} = \frac{-h_{21}}{h_{22}+1/r_L}$$ (See Eq. iii)

Putting this value in Eq. (vii)

$$A_v = \frac{-h_{21}}{\left(h_{22}+\frac{1}{r_L}\right).Z_{in}}$$

Substituting the values in h-parameters in CE configuration

$$A_v = \frac{-h_{fe}}{(h_{oe}+1/r_L).Z_{in}}$$

Power Gain (P_i). Power gain can be found by the product of current and voltage gains.

Power gain = current gain x voltage gain

Output admittance. The output impedance can be determined by using two assumptions $Z_L = \infty$ and $V_s = 0$.

Y_0 is defined as i_2/v_2 with $z_l = \infty$

But $$i_2 = h_f i_1 + h_0 v_2$$

Dividing by v_2

$$\frac{i_2}{v_2} = Y_0 = \frac{h_f i_1}{V_2} + h_0 \qquad (1)$$

From the equivalent circuit with $V_s = 0$,

$$r_s i_1 + h_i i_1 + h_f V_2 = 0$$

Here r_s = internal resistance of the source

V_s = open circuit signal voltage

Dividing by V_2 through out, we get

$$\frac{r_s i_1}{v_2} + \frac{h_i i_1}{V_2} + h_r = 0$$

or $$\frac{i_1}{V_2} = \frac{-h_r}{h_i + r_s} \qquad (2)$$

Substitute this value in the equation for Y_0 or equation (1)

$$Y_0 = h_f\left(\frac{-h_r}{h_i + r_s}\right) + h_0$$

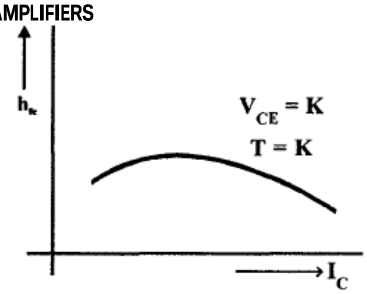
$\therefore$ $$Y_0 = h_0 - \frac{h_f h_r}{h_i + r_s}$$

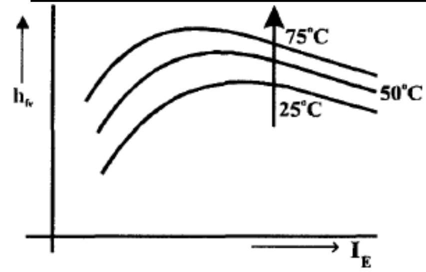
HYBRID PARAMETER VARIATIONS

When 'Q' the operating point is given, from input and output characteristics of the given transistors, we can determine the h-parameters. Conversely if the operating point is changing, the 'h' parameters will also change. I_C changes with temperature.

Hence 'h' parameters of a given transistor also change with temperature because the output and input characteristics change with temperature . Hence when the manufactures specify typical h-parameters for a given transistor, they also specify the operating point and temperature.

h_{fe} the small signal current amplification factor is very sensitive to I_C. Its variations is as shown in figure. The variation of h_{fe} with I_C and Temperature T are shown in figure above.





Limitations of h-parameters

- It is very difficult if not impossible to get accurate values of h-parameters for a transistor. The reason is that the h-parameters are subject to variations due to temperature, operating point and from unit to unit.
- A transistor behaves as a "two port" network for small signals only, hence h-parameters can be used to analyze only the small signal (i.e. single stage amplifiers).

Example

The h-parameters of a transistor in CE configurations are:

$h_{ie} = 1000\ \Omega$, $h_{re} = 3.5 \times 10^{-4}$, $h_{fe} = 55$, *and* $h_{oe} = 20\ \mu$ *mho*

If the load $r_L = 2$ *K, find current and voltage gains.*

Solution

(i) $$A_i = \frac{h_{fe}}{1 + h_{oe}.r_L} = \frac{55}{1 + (20x10^{-6}.2x10^3)} = 52.88$$

(ii) For finding voltage gain, first we find Z_{in}.

$$Z_{in} = h_{ie} - \frac{h_{re} x h_{fe}}{h_{oe} + 1/r_L} = 1000 - \frac{(3.5x10^{-4})x55}{(20x10^{-6}) + 1/(2x10^3)} = 962.98$$

Now, keeping the value of Z_{in} in the expression

$$A_v = \frac{-h_{fe}}{(h_{oe} + 1/r_L).Z_{in}} = \frac{-55}{[(20x10^{-6}) + 1/(2x10^3)]x962.8} = -112.2$$

The negative sign shows the 180^0 phase reversal between input and output.

Problem

Following figure shows the circuit of a single stage CE amplifier.

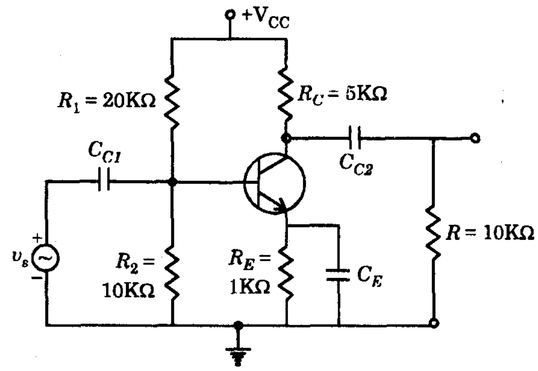
The values of h-parameters are $h_{ie} = 1.5\ k\Omega$, $h_{re} = 5 \times 10^{-3}$, $h_{fe} = 50$, $h_{oe} = 2 \times 10^{-5}\ \mu A/V$. *Determine the following*

(i) Current gain

(ii) Input resistance

(iii) *Voltage gain*

(iv) *Output resistance*



Answer: $A_i = -50$, $R_i = 1.5\ k\Omega$, *Input resistance* $Z_i = R_i||(R_1||R_2) = 1.22\ k\Omega$, $A_v = -110$, $R_o = 50\ k\Omega$, *Output resistance* $Z_o = R_o/R_L = 3.1\ k\Omega$

Hint: $R_L = R_C||R = 5||10 = 3.3\ k\Omega$

Problem

Find the values of voltage gain, current gain, input resistance and power gain for a common emitter transistor amplifier with $R_L = 1600$ *ohm and* $R_s = 1\ k\Omega$*. The transistor has* $h_{ie} = 1100$ *ohm,* $h_{fe} = 2.5 \times 10^{-4}$, $h_{oe} = 25\ \mu A/V$.

Answer: $A_v = -3.49 \times 10^{-4}$, $A_i = -2.4 \times 10^{-4}$, $R_i = 1100$ *ohm, power gain* $= A_iA_v = 8.37 \times 10^{-8}$

Example

For the emitter follower (CC amplifier) with $R_s = 0.5\ k\Omega$ *and* $R_L = 5\ k\Omega$*, calculate* A_i, R_i, A_v*. Assume* $h_{fe} = 50$, $h_{ie} = 1\ k\Omega$, $h_{oe} = 25\ \mu A/volt$.

Solution

(i) Current gain

$$A_i = \frac{1+h_{fe}}{1+h_{oe}R_L} = \frac{1+50}{1+25x10^{-6}x5x10^{3}} = 45.33$$

(ii) Input resistance

$$R_i = h_{ic} + h_{rc}A_iR_L$$

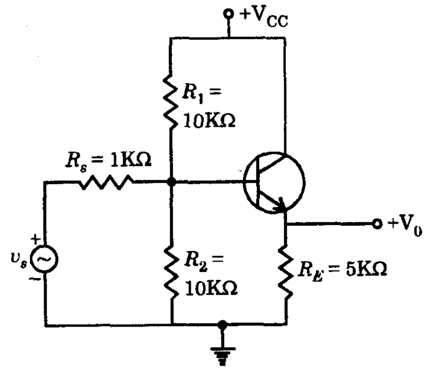
$$R_i = h_{ic} + 1.A_iR_L = h_{ie} + A_iR_L$$

$$R_i = 1x10^{3} + 45.33x5x10^{3} = 228.6\,k\Omega$$

(iii) $$A_v = \frac{v_o}{v_i} = \frac{A_iR_L}{R_i} = \frac{45.33x5}{227.6} = 0.9958$$

Problem

Following figure shows the circuit of common collector amplifier or emitter follower. The h parameters are h_{ic} = 2 kΩ, h_{fc} = -51, h_{rc} = 1 and h_{oc} = 25 x 10^{-6} mho. Determine the following (i) current gain (ii) input resistance (iii) voltage gain (iv) output resistance.



Answer: A_i = 45.3, R_i = 228 kΩ, Z_i = 4.9 kΩ, A_v = 1, R_0 = 58.8 Ω, Z_o = 581.1 Ω

Example

A BJT has h_{ie} = 2 kΩ, h_{fe} = 100, h_{re} = 2.5 x 10^{-4} and h_{oe} = 25 μA/V as parameters in CE configuration. It is used as an emitter follower (CC amp.) with R_s = 1 kΩ and R_L = 500 Ω. Determine for the amplifier, the voltage gain A_{Vs} = V_o/V_s, the current gain A_{is} = I_o/I_s, the input resistance R_i and output resistance R_o.

Solution

For the emitter follower (i.e. common-collector amplifier) transistor parameters are given as under:

$$h_{ic} = h_{i.e.} = 2\ k\Omega$$

$$h_{fc} = -(1 + h_{fe}) = -(1 + 100) = -101$$

$$h_{rc} = 1 - h_{re} = 1 - 2.5 \times 10^{-4} = 0.99975 = 1$$

$$h_{oc} = h_{oe} = 25 \times 10^{-6}$$

Current gain $A_i = \frac{-h_{fc}}{1+h_{oc}R_L} = \frac{-101}{1+25x10^{-6}(500)} = 99.75$

Input resistance

$$R_{in} = h_{ic} - \frac{h_{rc}h_{fc}}{h_{oc} + \frac{1}{R_L}} = 2x10^3 - \frac{1x(-101)}{25x10^{-6} + \frac{1}{500}} = 51.876\,k\Omega$$

Voltage gain $A_v = \frac{-h_{fc}}{\left(h_{oc} + \frac{1}{R_L}\right)R_{in}} = \frac{-(-101)}{\left(25x10^{-6} + \frac{1}{500}\right)x51.876x10^3} = 0.9614$

Overall voltage gain

$$A_{vs} = A_v \frac{R_{in}}{R_{in} + R_s} = 0.9614.\frac{51.876}{51.876 + 1} = 0.9432$$

Overall current gain

$$A_{is} = A_i \frac{R_s}{R_{in} + R_s}$$

$$A_{vs} = 99.75.\frac{1}{51.876 + 1} = 1.886$$

Output conductances

$$G_o = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ic} + R_s} = 25x10^{-6} - \frac{(-101x1)}{2x10^3 + 1x10^3} = 33.69x10^{-3}$$

Output resistance

$$R_o = \frac{1}{G_o} = \frac{1}{33.69x10^{-3}} = 29.68\Omega$$

Example

For a common emitter configuration, what is the maximum value of R_L for which R_i differs by no more than 10% of its value at $R_2 = 0$?

$h_{ie} = 1100\Omega$; $h_{fe} = 50$; $h_{re} = 2.50 \times 10^{-4}$; $h_{oe} = 25\ \mu℧$

Solution

Expression for R_i is

$$R_i = h_{ie} = -\frac{h_{fe}.h_{re}}{h_{oe} + \frac{1}{R_L}}$$

If $R_L = 0$, $R_i = h_{fe}$. The value of R_L for which $R_i = 0.9h_{ie}$ is found from the expression

$$0.9h_{ie} = h_{ie} - \frac{h_{fe}.h_{re}}{h_{oe} + \frac{1}{R_L}}$$

or $$\frac{h_{fe}.h_{re}}{h_{oe} + \frac{1}{R_L}} = h_{ie} - 0.9h_{ie} = 0.1h_{ie}$$

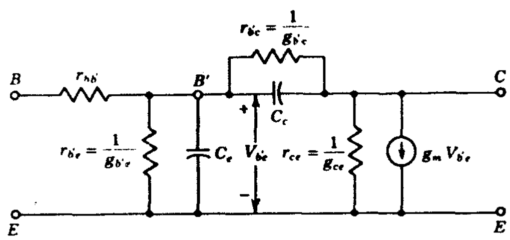
$$\frac{h_{fe}.h_{re}}{0.1h_{ie}} = h_{oe} + \frac{1}{R_L}$$

$$\frac{1}{R_L} = \frac{h_{fe}.h_{re}}{0.1h_{ie}} - h_{oe} = \frac{h_{fe}h_{re} - 0.1h_{oe}h_{ie}}{0.1h_{ie}}$$

or
$$R_L = \frac{0.1h_{ie}}{h_{fe}h_{re} - 0.1h_{oe}h_{ie}} = \frac{0.1x1100}{50\,x\,2.5\,x10^{-4} - 0.1x1100\,x\,25\,x10^{-6}} = 11.3k\Omega$$

HIGH FREQUENCY CE TRANSISTOR HYBRID π (II) MODEL

Earlier it has been emphasized that the common emitter circuit is the most important configuration. Hence we now seek a CE model which will be valid at high frequencies. A hybrid π(II) model is indicated in figure. The resistive components in this circuit can be obtained from the low-frequency h parameters.



The hybrid π model for a transistor in CE configuration

Circuit Components

The internal node B' is not physically accessible. The ohmic base-spreading resistance $r_{bb'}$ is represented as a lumped parameter between the external base terminal and B'.

For small changes in the voltage $V_{b'e}$ across the emitter junction, the excess minority carrier concentration injected into the base is proportional to $V_{b'e}$, and therefore the resulting small-signal collector current, with the collector shorted to the emitter, is proportional to $V_{b'e}$. This effect accounts for the current generator $g_mV_{b'e}$ in above figure.

The increase in minority carriers in the base results in increased recombination base current, and this effect is taken into account by inserting a conductance $g_{b'e}$ between B' and E. The excess-minority-carrier storage in the base is accounted for by the diffusion capacitance C_e connected between B' and E.

The varying voltage across the collector-to-emitter junction results in base-width modulation. A change in the effective base width causes the emitter(and hence collector) current to change because the slope of the minority carrier distribution in the base changes. This feedback effect between output and input is taken into account by connecting $g_{b'c}$ between B' and C. The conductance between C and E is g_{ce}.

Finally, the collector-junction barrier capacitance is included in C_c. Sometimes it is necessary to split the collector-barrier capacitance in two parts and connect one capacitance between C and B' and another between C and B. The last component is known as overlap-diode capacitance.

Hybrid π Conductances in Terms of Low-Frequency h-Parameters

If the CE h parameters at low frequencies are known at a given collector current I_C, the conductances or resistances in the hybrid π circuit are calculable from the following :

$$g_m = \frac{|I_C|}{V_T}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} \text{ or } g_{b'e} = \frac{g_m}{h_{fe}}$$

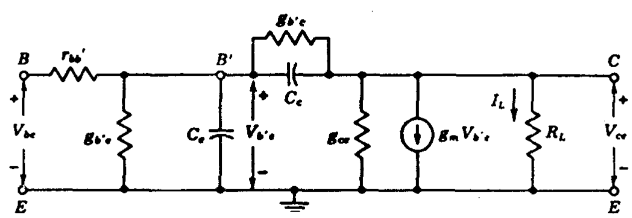
$$r_{bb'} = h_{ie} - r_{b'e} \qquad \text{(i)}$$

$$r_{b'c} = \frac{r_{b'e}}{h_{re}} \text{ or } g_{b'c} = \frac{h_{re}}{r_{b'e}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) g_{b'c} = \frac{1}{r_{ce}}$$

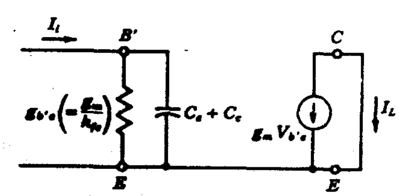
CE Short Circuit Current Gain Obtained with Hybrid π Model

Consider a single stage CE transistor amplifier. The load R_L on this stage is the collector circuit resistor, so that $R_c = R_L$. Let us assume that $R_L = 0$. To obtain the frequency response of the transistor amplifier, we use the hybrid π(II) model of figure, which is repeated for convenience in figure.



The hybrid π circuit for a single transistor with a resistive load R_L

The approximate equivalent circuit from which to calculate the short-circuit current gain is shown in figure below.



Approximate equivalent circuit for calculation of short circuit CE current gain

A current source furnishes a sinusoidal input current of magnitude I_i, and the load current is I_L. We have neglected $g_{b'c}$, which should appear across terminals B'C, because $g_{b'c} << g_{b'e}$. And of course g_{ce} disappears because it is in shunt with a short circuit. An additional approximation is involved, in that we have neglected the current delivered directly to the output through $g_{b'c}$ and C_c.

The load current is $I_L = -g_m V_{b'e}$, where

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)} \qquad \text{(ii)}$$

The current amplification under short-circuited conditions is

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)} \qquad \text{(iii)}$$

Using the results given in equation (i), we have

$$A_i = \frac{-h_{fe}}{1 + j(f / f_\beta)} \qquad \text{(iv)}$$

where the frequency at which the CE short-circuit gain falls by 3 dB is given by

$$f_\beta = \frac{g_{b'e}}{2\pi(C_c + C_e)} = \frac{1}{h_{fe}} . \frac{g_m}{2\pi(C_e + C_c)} \qquad \text{(v)}$$

The frequency range up to f_β is referred to as bandwidth of the circuit.

The parameter f_T. We introduce now f_T, which is defined as the frequency at which the short-circuit common-emitter current attains unit magnitude.

Since $h_{fe} >> 1$, we have, from eqn. (iv) and (v) that f_T is given by

$$f_T \approx h_{fe} . f_\beta = \frac{g_m}{2\pi(C_e + C_c)} \approx \frac{g_m}{2\pi C_e} \qquad \text{(vi)}$$

since $C_e >> C_c$. Hence from Eq. (iv)

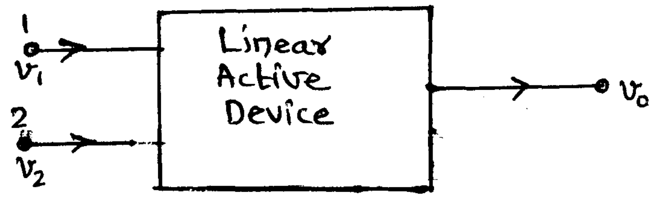
$$A_i \approx \frac{-h_{fe}}{1 + jh_{fe}(f / f_T)} \qquad \text{(vii)}$$

The parameter f_T is an important high frequency characteristic of a transistor. Like other transistor parameters, its value depends on the operating conditions of the device.

Since $f_T \approx h_{fe}.f_\beta$, this parameter may be given a second interpretation. It represents the *short circuit current gain bandwidth* product; that is, for the CE configuration with the output shorted, f_T is the product of the low frequency current gain and the upper 3 dB frequency.

DIFFERENCE AMPLIFIER

The function of a difference, or differential amplifier is to amplify the difference between two signals. Figure below represents a linear active device with two input signals v_1, v_2 and one output signal v_0, each measured with respect to ground.



In an ideal differential amplifier the output signal v_0 should be given by

$$v_0 = A_d(v_1 - v_2) \qquad \text{(i)}$$

where A_d is the gain of the differential amplifier. However, a practical differential amplifier cannot be described by Eq. (i) since, in general, the output depends not only upon the difference signal v_d of the two signals, but also upon the average level, called the **common mode signal v_c**, where

$$v_d = v_1 - v_2 \quad \text{and} \quad v_c = (1/2)(v_1 + v_2) \qquad \text{(ii)}$$

The Common-mode Rejection Ratio(CMRR)

The foregoing statements are now clarified, and a figure of merit for a difference amplifier is introduced. The output of above figure can be expressed as a linear combination of the two input voltages

$$v_0 = A_1v_1 + A_2v_2 \qquad \text{(iii)}$$

where $A_1(A_2)$ is the voltage amplification from input 1(2) to the output under the condition that input 2(1) is grounded. From Eqs (ii)

$$v_1 = v_c + (1/2)v_d \quad \text{and} \quad v_2 = v_c - (1/2)v_d \qquad \text{(iv)}$$

if these equations are substituted in Eq. (iii), we obtain

$$v_0 = A_dv_d + A_cv_c \qquad \text{(v)}$$

where

$$A_d = (1/2)(A_1 - A_2) \quad \text{and} \quad A_c = A_1 + A_2 \qquad \text{(vi)}$$

Clearly, we should like to have A_d large, whereas, ideally, A_c should equal zero. A quantity called the **common-mode rejection ratio**, which serves as a figure of merit for a difference amplifier, is

$$\rho = \left|\frac{A_d}{A_c}\right| \qquad \text{(vii)}$$

From above equations, we obtain an expression for the output in the following form:

$$v_0 = A_d v_d \left(1 + \frac{1}{\rho}\frac{v_c}{v_d}\right) \qquad \text{(viii)}$$

Example

Consider the situation referred to above where the first set of signals is v_1 = + 50μV and v_2 = - 50μV and the second set is v_1 = 1050μV and v_2 = 950μV. If the common-mode rejection ratio is 100, calculate the percentage difference in output voltage obtained for the two sets of input signals.

Solution

In the first case, $v_d = 100\mu V$ and $v_c = 0$, so that, from Eq. 44, $v_0 = 100A_d\mu V$.

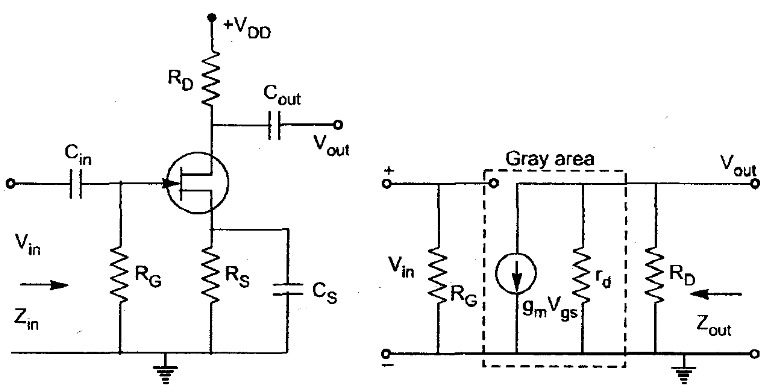
In the second case, $v_d = 100\mu V$, the same value as in part a, but now $v_c = (1/2)(1050 + 950) = 1000\ \mu V$, so that, from Eq. (viii),

$$v_o = 100A_d\left(1+\frac{10}{\rho}\right) = 100A_d\left(1+\frac{10}{100}\right)\ \mu V$$

These two measurements differ by 10%.

COMMON SOURCE FET AMPLIFIER

Following figure (a) shows the circuit diagram of a common source FET amplifier and the figure (b) shows the corresponding equivalent circuit with appropriate labelling.



(a) **(b)**

In drawing the equivalent circuit, the battery V_{DD} is replaced by a short circuit and $X_{C,in}$ and $X_{C,out}$ are considered as short circuits. Further C_s is used for bypassing the a.c. signal and $X_{cs} = 0\ \Omega$.

We get

Input resistance

$$Z_{in} = R_G$$

Output resistance

$$Z_{out} = R_d \,||\, r_d = \frac{R_d r_d}{R_d + r_d}$$

If $r_d \geq 10R_D$

then $Z_{out} \approx R_D$

The expression for voltage gain is

$$G_V = \frac{V_{out}}{V_{gs}}$$

$$V_{out} = I_d \cdot \frac{R_D r_d}{R_D + r_d}$$

also $V_{gs} = \frac{I_d}{g_m}$

Thus $G_V = I_d \cdot \frac{R_D r_d}{R_D + r_d} x \frac{g_m}{I_d} = g_m\left(\frac{R_D r_d}{R_D + r_d}\right)$

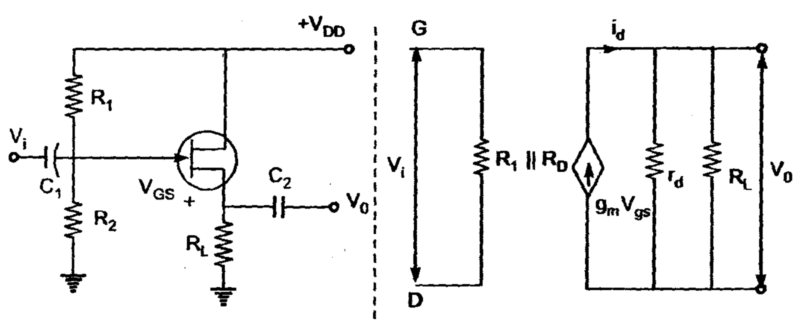
If $r_d \geq 10R_D$

then $G_V \approx g_m R_D$

The value of voltage gain for a common drain FET amplifier is less than 1.

COMMON DRAIN FET AMPLIFIER

In the common drain FET amplifier circuit also called source follower, the load resistance is in series with the source terminal. There is no drain resistor. Figure (a) and (b) shows a common drain FET amplifier and its equivalent circuit respectively.



(a) (b)

The input signal is applied to the gate through the capacitor C_1 and the output is taken out from the source via C_2. The current generator is $g_m V_{gs}$ where $V_{gs} = (V_i - V_o)$.

Voltage gain

$$V_o = i_d x(r_d \parallel R_L)$$

since $i_d = g_m V_{gs} = g_m(V_i - V_o)$

∴ $$V_o = g_m(V_i - V_o)x(r_d \parallel R_L) = g_m(V_i - V_o)\frac{r_d R_L}{r_d + R_L}$$

Solving for V_o, we get

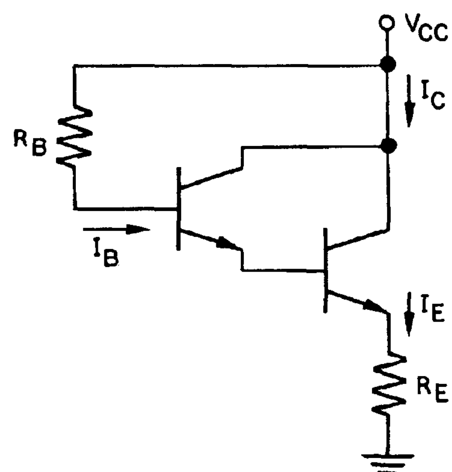
$$V_o = g_m V_i \frac{r_d R_L}{r_d + R_L + g_m r_d R_L}$$

∴ $$A_V = \frac{V_o}{V_i} = \frac{r_d R_L g_m}{r_d + R_L + g_m r_d R_L} \cong 1$$

if $$g_m R_L >> (r_d + R_L)$$

DARLINGTON PAIR

In some applications of amplifier circuits very high input impedance is required. To achieve this, the circuit shown in following figure called Darlington pair, is used. Darlington circuit consists of two cascaded emitter followers wherein second transistor constitutes the emitter load for the first as shown in figure. The current gain of such an arrangement is β^2, where β is the gain of individual transistor. The voltage gain of the pair is less than unity as each transistor is connected in emitter follower configuration.



Bias Analysis

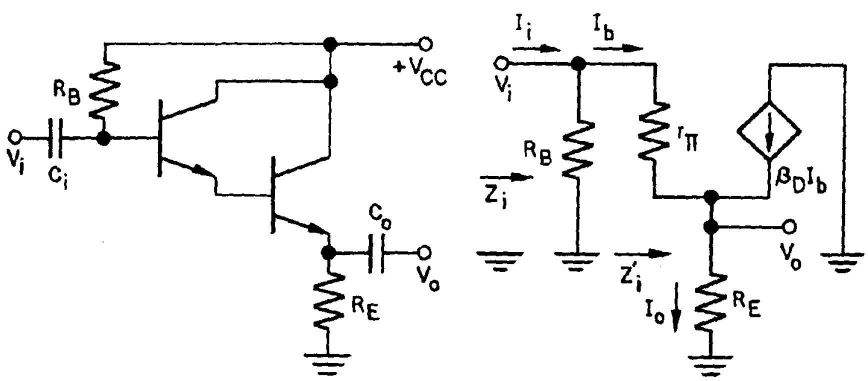
Let β_0 be the effective β of the pair and V_{BE} the effective base-emitter voltage (= twice that of each transistor). Then for bias conditions circuit analysis of above figure gives

$$V_{CC} - V_{BE} = R_B I_B + R_E I_E = R_B I_B + \beta_D R_E I_B; \text{as } \beta_D >> 1$$

or $$I_B = \frac{V_{CC} - V_{BE}}{(R_B + \beta_D R_E)}$$

AC Analysis

The circuit of the Darlington pair with coupling capacitors and ac input is shown in following figure(a). With C_i and C_o considered as short circuits in the midband, the circuit model for ac quantities is drawn in figure (b).



(a) (b)

Input Impedance

$$Z_i = r_\pi + \beta_D R_E$$

Current Gain

$$A_i = \frac{\beta_D R_B}{R_B + \beta_D R_E}$$

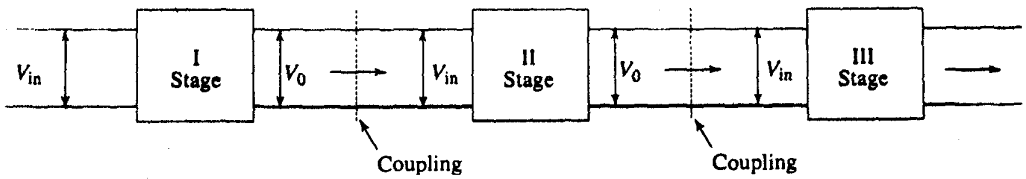
Voltage Gain

$$A_V = \frac{R_E}{r_\pi / B_D + R_E} \approx 1 \text{ as } r_\pi / \beta_D << R_E$$

Multistage Amplifiers

As already mentioned, output of a single stage amplifier is low. Therefore, all practical amplifiers are "multistage" i.e. they have more than one stage. The stages are connected(cascaded) with each other with some coupling device.

Each stage consists of one transistor and the associated circuitry. One stage is coupled to the next stage such that the output of one stage becomes automatically the input of next stage and so on. (Figure).



Multistage(cascaded) amplifier

The multistage amplifiers are named according to the coupling. In following table are listed the types of multistage amplifiers and the coupling used.

	Name of amplifier	Type of coupling
1	RC coupled amplifier	Resistance capacitance coupling
2	Transformer coupled amplifier	Transformer coupling
3	Direct coupled amplifier	No coupling

The **RC coupled amplifiers** use resistance/capacitance coupling between two stages. The capacitance does not allow D.C. components of the amplified output of the preceding stage to the next stage. These are basic amplifiers used as audio and video amplifiers(with some changes). They are used to amplify voltage of the signal in the first few stages of the amplifier systems.

The **transformer coupled** amplifiers use transformer as the coupling device. They perform two functions : (a) they block D.C. component and do not allow it to pass to the next stage. (b) They help in impedance matching with the load. It is to be mentioned here that these are used at the final stage of the amplification, where they are to be coupled with loudspeaker or the other load.

In **direct coupled amplifiers**, the successive stages are directly coupled to each other. These are used for amplifying very low frequency signal (up to 10 Hz) and therefore, do not need any coupling for by-passing D.C.

IMPORTANT TERMS

Important terms related to amplifiers are:

- Gain
- Frequency response
- Bandwidth

These are explained below :

Gain

The ratio of the output to the input of an amplifier is called gain. It may be:

Current gain, A_i = output current/input current = I_0/I_{in}

Voltage gain, A_v = output voltage/input voltage = V_0/V_{in}

Power gain, A_p = output power/input power = P_0/P_{in}

Generally, by the term "gain" of an amplifier we mean its voltage gain, which is represented by G or A.

Absolute gain : The gain of an amplifier, when specified in number is called its "absolute gain". The gain of a multistage amplifier is equal to the product of the gains of its individual stages.

$$G = G_1.G_2.G_3\ldots..G_n.$$

Thus the total gain of an amplifier is equal to the product of the gains of its various stages. The gain in number is called "absolute gain".

If an amplifier has three stages having gains as 2, 3 and 4, respectively, its total gain will be equal to 2 x 3 x 4 = 24.

Decibel gain : Though the gain of amplifier is generally given in number, but practically it is useful to designate the gain in "bel" or "decibel".

$$P.G. = \log_{10}\left(\frac{P_0}{P_{in}}\right) bel$$

The more convenient unit and which is used more frequently is decibel or dB and i bel = 10 dB. Now we shall find expressions for power, voltage and current gains in dB.

$$\text{dB power gain} = A_p = 10\log\left(\frac{P_0}{P_{in}}\right)$$

$$\text{dB voltage gain}, A_v = 20\log_{10}\frac{V_0}{V_{in}} = 20\log_{10} V_0/V_{in}$$

$$\text{dB current gain} = A_i = 20\log_{10} I_0/I_{in}$$

Upper band limit of each stage in cascaded amplifier. A cascaded (multistage) amplifier (n-stage) can be represented by the block diagram as shown below. it may be noted that the output of the first stage makes the input of the second stage, the output of the second stage makes the input of third stage and so on.

The signal voltage V_s is applied to the input of the first stage. The final output V_0 is then available at the output terminals of the last stage.

The high 3-dB frequency for n-cascaded stages is f_H and equal lo the frequency for which the overall voltage gain falls 3 dB i.e. $1/\sqrt{2}$ of its mid band value. To obtain the overall transfer function of non-interacting stages, the transfer gain of individual stages are multiplied together.

Hence, if each stages has a dominant pole and if the high 3-dB frequency of its stage is f_{H1} where i = 1. 2, 3, ... n, then f_{H*} can be calculated from the product.

$$\frac{1}{\sqrt{1+\left(\frac{f_{H*}}{f_{H1}}\right)^2}}\cdots\frac{1}{\sqrt{1+\left(\frac{f_{H*}}{f_{H2}}\right)^2}}\cdots\frac{1}{\sqrt{1+\left(\frac{f_{H*}}{f_{Hn}}\right)^2}}=\frac{1}{\sqrt{2}}$$

for n stages with identical upper 3dB frequencies, we have

$$f_{H1}=f_{H2}=\cdots f_{Hi}=f_{Hn}=f_H$$

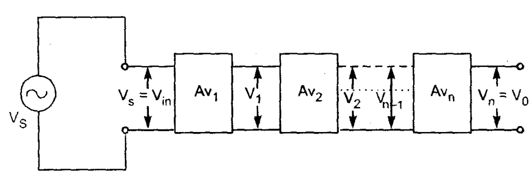
Hence f_{H*} is calculated as

$$\left[\frac{1}{\sqrt{1+\left(\sqrt{\frac{f_{H*}}{f_H}}\right)^2}}\right]^n=\frac{1}{\sqrt{2}}$$

or $$f_{H*}=f_H\sqrt{2^{1/n}-1}$$

or $$f_H=\frac{f_{H*}}{\sqrt{2^{1/n}-1}}$$

Voltage gain of Cascaded Amplifier. Let us consider following cascaded amplifier of n stages.



The signal voltage v_s is applied to the input of the first stage. The final output v_0 is then available at the output terminals of the last stage. The output of the first stage or the input of the second stage is

$$v_1=A_{v1}v_s$$

where A_{v1} is the voltage gain of the first stage. Then the output of the second stage (or the input to the third stage) is

$$v_2=A_{v2}v_1$$

Similarly, the final output v_0 is given as

$$v_0=v_n=A_{vn}v_{n-1}$$

where A_{vn} is the gain of the nth stage.

Now overall gain A_V of the multistage amplifier is given as

$$A_v = \frac{v_0}{v_s} = \frac{v_1}{v_2} = \frac{v_2}{v_1} x.......... \frac{v_{n-1}}{v_{n-2}} x \frac{v_0}{v_{n-1}}$$

$$A_v = A_{v1} x A_{v2} x A_{v3} x...... A_{n-1} x A_n$$

The overall voltage gain in dB of a multistage amplifier is the sum of the decibel voltage gains of the individual stages i.e.

$$20\log_{10} A = 20\log_{10} A_1 + 20\log_{10} A_2 + ... + 20\log_{10} A_n$$

or $$A_{dB} = A_{db1} + A_{dB2} + A_{dB3} + ... A_{dBn}$$

The value of n can not be increased indefinitely, because as n increases, then bandwidth of multistage amp decreases.

Frequency Response

The way in which an amplifier responds to the different frequencies of the input signal is called its frequency response.

In other words, the variation of the voltage gain of an amplifier with respect to the signal frequency may be defined as "frequency response" of the amplifier. The reactance of the capacitors connected in an amplifier varies with the frequency ($X_C \propto 1/f$); hence, the gain of the amplifier also varies.

Band Width

The range of frequencies for which the gain of an amplifier is equal to or greater than 70.7% of the maximum gain is called its bandwidth. In other words the frequency range from low frequency(f_1) to high frequency(f_2) is called "bandwidth" of the amplification stage.

Example

A three stage amplifier has a gain of its three stages as 40, 50, and 60 respectively. Find the total gain of the system. Express the gain also in dB.

Solution

(a) Total gain of the system

$$G = G_1 x G_2 x G_3 = 40x50x60 = 12x10^4$$

(b) Total gain in dB

$$= 20\log_{10}(12x10^4) = 101.6\,\text{dB}$$

Example (AMIE S08, 6 marks)

A single stage CE amplifier has lower 3 dB cut off of 64 Hz and an upper 3 dB cut off of 10 kHz. What will be the new value for these frequencies for two stage amplifier consisting of a cascaded arrangement of two identical stages of the type mentioned.

Solution

We know $$f_{1n} = \frac{f_1 \, per\ stage}{\sqrt{(2^{1/n} - 1)}}$$

and $$f_{2n} = f_2 \ per\ stage\ x \sqrt{2^{1/n} - 1}$$

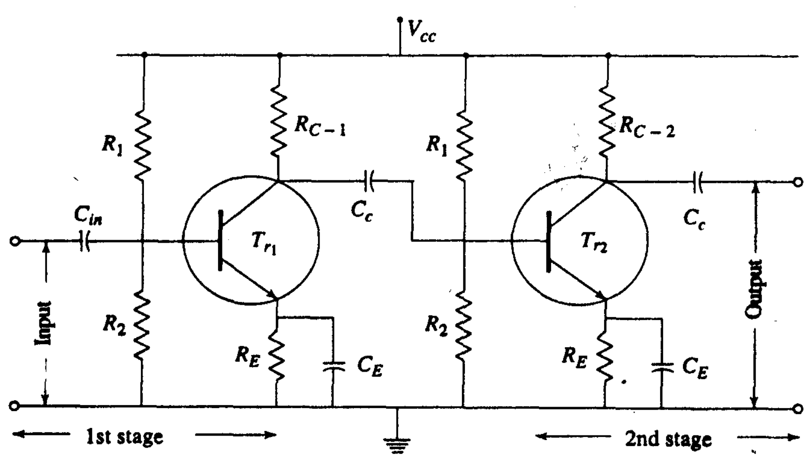
Putting n = 2, f_1 = 64 Hz, f_2 = 10 kHz

We have $$f_{12} = \frac{64}{\sqrt{2^{1/2} - 1}} = 100 Hz$$

$$f_{22} = \frac{10\, x 10^3}{1} x \sqrt{2^{1/2}} = 64.34 kHz$$

RC COUPLED AMPLIFIER

Figure below shows a two stage RC coupled amplifier. In the same way any number of stages can be interconnected by a coupling capacitor(C_C) followed by a connection to a shunt resistor. Hence the name. This is usually employed as a voltage amplifier. You may recall that the capacitor connected at the input of the amplifier acts as blocking capacitor (C_b) and the capacitor connected in between the stages acts as coupling capacitor (C_c).



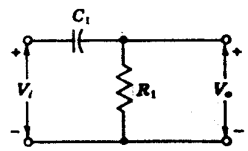
An RC Coupled Amplifier

Operation

When A.C. signal is given at the input of the first stage, it is amplified and the output can be obtained across R_{C1}. This amplified output is passed to the second stage, which further amplifies it. Thus the signal passes through successive stages and the amplified output is obtained across R_C of the last stage.

Low Frequency Response

Video amplifiers are almost invariably of RC coupled type. For such a stage the frequency characteristics may be divide into three regions: There is a range, called the **midband frequencies**, over which the amplification is reasonably constant and equal to A_0 and over which the delay is also quite constant.



A high pass RC circuit may be used to calculate low frequency response of an amplifier

For the present discussion we assume $A_0 = 1$. In the second (low frequency) region, below the midband, an amplifier stage behaves like the simple high-pass circuit of figure 3 of time constant $\tau_1 = R_1C_1$. From this circuit we find that

$$V_0 = \frac{V_i R_1}{R_1 - j/\omega C_1} = \frac{V_i}{1 - j/\omega R_1 C_1}$$

The voltage gain at low frequencies A_1 is defined as the ratio of the output voltage V_0 to the input voltage V_i, or

$$A_1 = \frac{V_0}{V_i} = \frac{1}{1 - jf_1/f}$$

where $$f_1 \equiv \frac{1}{2\pi R_1 C1}$$

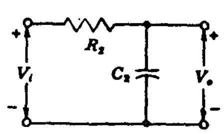
The magnitude $|A_1|$ and the phase lag θ_1 of the gain are given by

$$|A_1| = \frac{1}{\sqrt{1+(f_1/f)^2}}, \theta_1 = -\arctan\frac{f_1}{f}$$

At frequency $f = f_1$, $A_1 = 1/\sqrt{2} = 0.707$, whereas in the midband region ($f>>f_1$), $A_1 \rightarrow 1$. Hence f_1 is that frequency at which the gain has fallen to 0.707 times its midband value A_0.

High Frequency Response

In the third (high frequency) region, above the midband, the amplifier stage behaves like simple low pass circuit of following figure , with a time constant $\tau_2 = R_2C_2$.



A low pass RC circuit may be used to calculate high frequency response of amplifier

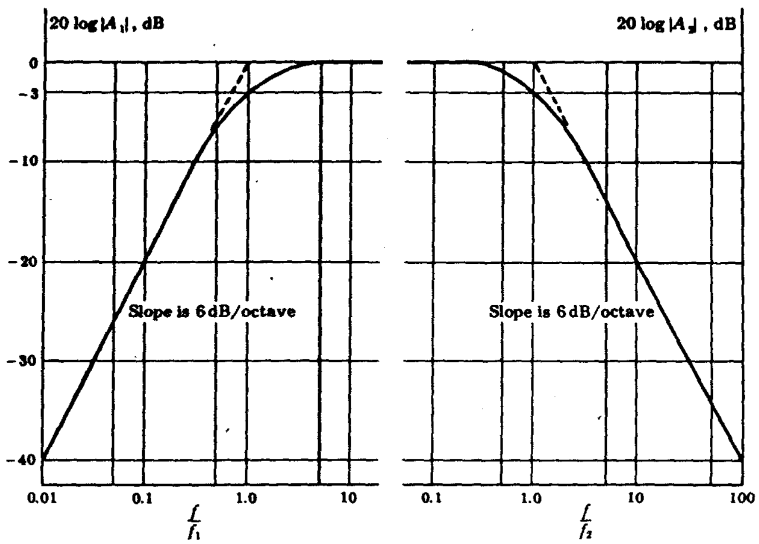
Proceeding as above, we obtain for the magnitude $|A_2|$ and the phase lag θ_2 of the gain

$$|A_2| = \frac{1}{\sqrt{1+(f/f_2)^2}}, \theta_2 = \arctan\frac{f}{f_2}$$

where $f_2 = \frac{1}{2\pi R_2 C_2}$

Since at f = f_2 the gain is reduced to $1/\sqrt{2}$ times its midband value, then f_2 is called the upper **3-dB frequency**. It also represents that frequency for which the resistance R_2 equals the capacitive reactance $1/2\pi f_2 C_2$. In the above expressions θ_1 and θ_2 represent the angle by which the output lags the input, neglecting the initial 180^0 phase shift through the amplifier.

The frequency dependence of the gains in the high and low frequency range is shown in figure below.



Frequency response characteristic of an RC coupled amplifier

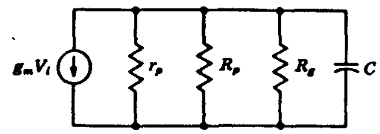
We see that at low frequencies (below 50 Hz) the gain is small and it does not allow the signal to pass from one stage to the next. Moreover, at low frequencies C_E also offers high reactance and can not "shunt" R_E effectively and therefore some feedback occurs, which reduces the gain.

At mid frequency (50 Hz – 20 kHz) the gain of the amplifier remains almost constant; because of this frequency the reactance of C_c is decreased.

At high frequencies(> 20 kHz), the voltage gain of the amplifier again decreases, as the value of capacitive reactance decreases. Thus, it behaves as a short circuit which increases the loading effect of the next stage.

Gain Bandwidth Product

Consider high frequency model of RC coupled stage using a pentode (Figure).



High frequency model of an RC coupled stage using a pentode

The upper 3-dB frequency of the amplifier may be given by

$$f_2 = \frac{1}{2\pi R_p C}$$

Also, Figure of merit

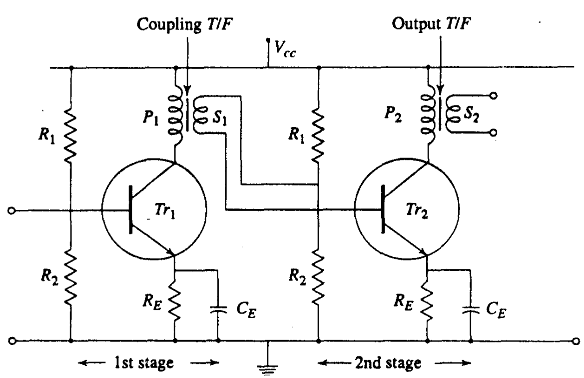
$$F = |A_0| f_2$$

$F = |A_0| f_2$ is called the gain bandwidth product. It should be noted that f_2 varies inversely with plate circuit resistance, whereas A_0 is proportional to R_p so that the gain bandwidth product is a constant independent of R_p. It is possible to reduce R_p to such a low value that a midband gain $|A_0| = 1$ is obtained. Hence the figure of merit F may be interpreted as giving the maximum possible bandwidth obtainable with a given tube if R_p is adjusted for unity gain.

TRANSFORMER COUPLED AMPLIFIER

Given figure shows a two stage transformer coupled amplifier. This is similar to that of an RC coupled amplifier except that the successive stages are coupled by a transformer. The coupling transformer performs the following functions:

- It transfers the output of one stage to the next.
- It helps in impedance matching. This is the reason that these are employed at the final stage of an amplifier system.
- The transformer also reduces the loading effect. In this way the voltage(or power gain) of this amplifier is improved as compared to the RC amplifier.



Transformer coupled amplifier

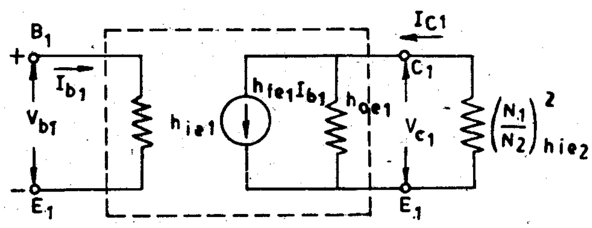
Operation

A transformer coupled amplifier is generally used for power amplification as it is connected at the final stage with a load usually (a loudspeaker). These amplifiers however handle small powers. As can be seen the primary(P) of the transformer acts as collector load(R_C) and output to the next stage is given through the secondary.

When AC signal is applied at input of the first stage, it is amplified by the transistor Tr_2 and the amplified output appears across primary(P_1) of the transformer. Now by the transfer action (electro magnetic induction) the output is transferred to the secondary (S_1) which becomes the input of the next stage and so on. From the secondary of the final stage the output is taken across a load usually a loudspeaker.

Stage Current Gain & Voltage Gain

Consider figure.



To determine the current gain assume I_{b1} flowing into B_1 as shown in figure above. The transistor current generator is $h_{fe1}I_{b1}$ so the collector current I_{c1} through the transformer primary will be $h_{fe1}I_{b1}/2$ for the matched conditions.

Since T_2 is a step down transformer, the expression for I_{b2} becomes $I_{b2} = (N_1/N_2)I_{c1} = (N_1/N_2)(h_{fe}I_{b1}/2)$ and the current gain $A_i = I_{b2}/I_{b1} = \frac{N_1}{N_2}.\frac{h_{fe1}}{2}$.

The stage voltage gain A_v is given by V_{b2}/V_{b1}.

$$V_{c1} = -I_{c1}\left(\frac{N_1}{N_2}\right)^2 h_{ie2} \quad \text{and} \quad I_{c1} = h_{fe1}/2 \quad \text{and} \quad I_{b1} = V_{b1}/h_{ie1}$$

Hence $$\frac{V_{c1}}{V_{b1}} = \frac{-h_{fe1}}{2} x \frac{h_{ie2}}{h_{ie1}}\left(\frac{N_1}{N_2}\right)^2 \text{ but } \frac{V_{c1}}{V_{b2}} = \frac{-N_1}{N_2}$$

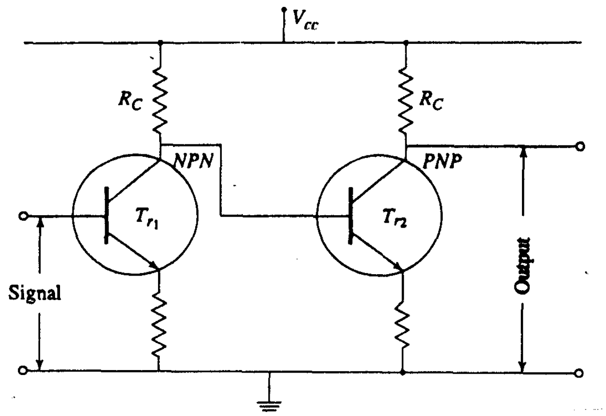
Hence $$A_V = \frac{h_{fe1}}{2} x \frac{h_{ie2}}{h_{ie1}} x \frac{N_1}{N_2}$$

If both the transistors are equal $h_{ie2} = h_{ie1}$

Hence $$A_V = \frac{N_1}{N_2} x \frac{h_{fe1}}{2}$$

DIRECTLY COUPLED AMPLIFIERS

In these amplifiers, no coupling device is used and the different stages are directly connected to each other through a simple wire. In these amplifiers, complementary transistors (e.g. N-P-N, then P-N-P, then again N-P-N and so on, are used. By using complementary transistors, the variations due to temperature, etc, can be compensated.



Directly Coupled Amplifiers

Operation

The signal to be amplified is given at the input of first stage. The amplified output is obtained across its R'_C. This output passes directly to the next stage and so on. The net output is obtained across R_C of the final stage.

Example

In a two-stage RC amplifier, each stage has R_{in} = 1 K, β = 100, R_C = 2 K.

Find : (i) Voltage gain of second stage (ii) voltage gain of first stage (iii) overall voltage gain of the amplifier in number as well as in dB.

Solution

(i) The voltage gain of second stage will remain unaffected due to absence of loading effect.

Hence voltage gain of second stage = $\beta(R_C/R_{in})$ = 100 x 2000/1000 = 200

(ii) Voltage gain of first stage will not be 200 but it will be reduced due to loading effect of the second stage.

Here, effective load $R_{AC} = R_C||R_{in} = R_C.R_{in}/(R_C+R_{in})$ = 2000 x 1000/(2000 + 1000) = 666.6 Ω

Hence Voltage gain of first stage = $\beta.R_{AC}/R_{in}$ = 100 x 666.66/1000 = 66.66

(iii) Hence overall gain of two stage amplifier = 200 x 66.66 = 13333.33

Gain in dB = 20 $\log_{10}$(13333.33) = 20 x 4.12 = 82.4 dB.

ASSIGNMENT

Q.1. (AMIE S05, W12, 10 marks): Define the hybrid equivalent parameters for BJT in a common emitter configuration. Find the expression for current gain and input resistance of the CE amplifier in terms of the hybrid parameters. Are the h-parameters for a transistor constant? What do they vary with?

Q.2. (AMIE S07, 13, W11, 8 marks): Define the four h-parameters for the small signal model of a bit at low frequency and give the analytical expression for each. Assume CE configuration.

Q.3. (AMIE S07, 14, 12 marks): Derive the current gain (A_I), amplification of voltage (A_v), input impedance (Z_i) and output admittance (Y_0) in terms of h parameters and load resistance Z_L. If the source resistance R_s is taken into account how will the voltage amplification factor change.

Q.4. (AMIE S10, 5 marks): Draw a neat sketch showing the variation of hybrid parameters h_{ib}, h_{rb}, h_{fb} and h_{ob} with emitter current.

Q.5. (AMIE W11, 8 marks): Using approximate hybrid π model for a single stage CE amplifier at high frequency, find the expression for current gain(A_i) anf f_T which is frequency at which $|A_i| = 1$.

Q.6. (AMIE S09, 6 marks): What is Darlington connection? Compare between an emitter follower and a Darlington pair.

Q.7. (AMIE S05, 06, 10 marks): Draw the circuit diagram for a common source FET amplifier and the corresponding equivalent circuit with appropriate labelling. Find expressions for voltage gain, output resistance in terms of FET parameters and circuit elements.

Q.8. (AMIE S10, 13, 5 marks): Show that the voltage gain of a CS amplifier is given by $A_V = -\mu R_D/(r_d + R_D)$

Q.9. (AMIE W05, 6 marks): Draw the common source drain FET amplifier and its equivalent circuit. Determine its voltage gain.

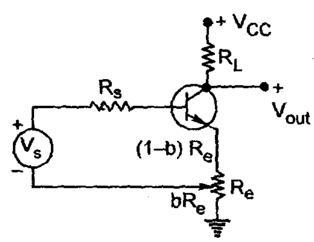
Q.10. (AMIE W07, 10 marks): For a single stage transistor amplifier operated at low frequency

$h_{ie} = 1100\ \Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 24\ \mu A/V$

(i) What is the maximum value of R_L for which R_i differs by not more than 10% of its value at $R_L = 0$.

(ii) What is the maximum value of R_s for which R_0 differs by not more than 10% of its value

Q.11. (AMIE W07, 10 marks): For the circuit shown in figure, find the voltage gain V_0/V_s as a function of R_s, b, R_e and R_L. Assume $h_{oe} = (R_e + R_L) \leq 0.1$



Answer: $A_v = \dfrac{-h_{fe}R_L}{(1+h_{fe})(1-b)R_e}$

MULTI STAGE AMPLIFIERS

Q.12. (AMIE W09, 6 marks): What are multistage amplifiers and where are they used? Draw a set of n-cascaded amplifiers and show that the overall voltage gain A_V can be expressed as

$$A_V = A_{V1}, A_{V2}, A_{V3}........A_{Vn}$$

where A_V's denote voltage gains of individual stages. Can this value of n be increased indefinitely? Give reasons for your answer.

Q.13. (AMIE W05, 6 marks): Discuss the effect of cascading multiple stages of amplifier sections over gain and bandwidth of the overall amplifier. Derive the expression for overall gain for n stage cascade system.

Q.14. (AMIE S10, 13, 5 marks): A multistage amplifier comprises N identical stages and has cutoff frequency of ω_0. Show that the upper band limit ω_2 of each stage is given by

$$\omega_2 = \omega_0 / \sqrt{2^{1/N} - 1}$$

Q.15. (AMIE S14, 6 marks): Draw the circuit of RC coupled amplifier. What are the components of this circuit that affect the bandwidth?

Q.16. (AMIE W14, 14 marks): Explain, with a neat circuit, the operation of an R-C coupled amplifier. Draw its gain frequency response. Using h-parameter analysis, explain why gain fells at low frequency region of operation and remains constant over mid-frequency range of operation.

Q.17. (AMIE W10, 10 marks): Using h-parameter analysis, explain why gain falls at low frequency but remains constant at mid frequency range for operation of an RC coupled amplifier.

Q.18. (AMIE S10, 4 marks): How do coupling and bypass capacitors affect the frequency response of an amplifier stage?

Q.19. (AMIE S05, 10 marks): With the help of suitable circuit, explain the effect of coupling and device capacitors on the frequency response of RC coupled BJT amplifier.

Q.20. (AMIE S09, 20 marks): Draw the circuit diagram of a two stage RC coupled CE transistor amplifier and explain its operation. Obtain an expression for the voltage gain of the RC coupled amplifier in the mid and high frequency ranges. Write down the assumptions as may be necessary for the derivation.

Q.21. (AMIE W12, 12 marks): With a neat circuit diagram, explain the operation of a two identical gain stage R-C coupled amplifier. Draw its gain-frequency response. Explain, using high frequency model analysis, why gain is constant over mid-frequency range and falls at low frequency region of operation. Derive an expression for overall bandwidth.

Q.22. (AMIE S14, 6 marks): Discuss the frequency response of multistage amplifiers. Calculate the overall upper and lower cut-off frequency for a 5-stage amplifier.

Q.23. (AMIE W06, 8 marks): What are the advantages of a transformer coupled amplifier? Find the overall voltage gain of a two stage transformer coupled amplifier in terms of the turns ratio of the coupling transformer.

Q.24. (AMIE W08, 15 marks): It is desired to have a low 3 dB frequency of not more than 10 Hz for an RC coupled amplifier for which R_C = 1 K. What is the minimum value of coupling capacitance required where transistors with h_{ie} = 1 K and $1/h_{oe}$ = 40 K are used. Also, $R_1 = R_2$ = 20 K. Derive the relation used.

Answer: 80 μF

Q.25. (AMIE W09, 14 marks): In a CE RC coupled amplifier, the total effective shunt capacitance in the input circuit, including the Miller effect component, is 300 pF. The hybrid π parameter r_{be} = 800Ω. Calculate the upper 3 dB frequency. At what frequency in the high frequency range will the voltage gain be below 6 dB of the mid-band gain?

Answer: 530.785 Hz